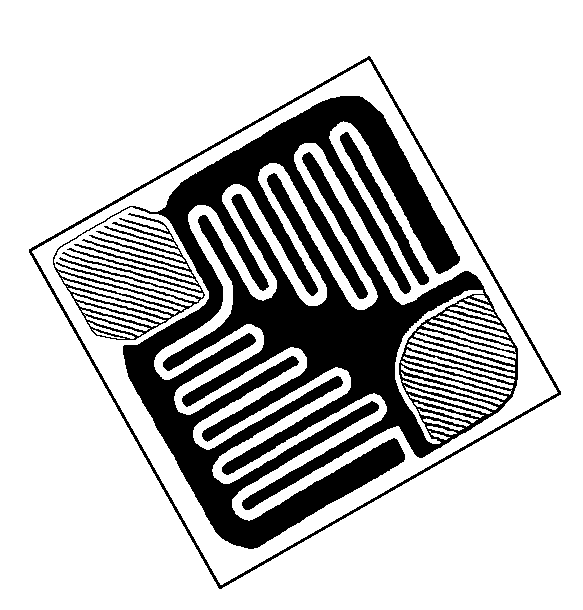
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**BASE**

**EMITTER**

**.020”**

**.020”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004” min**

**Backside Potential: COLLECTOR**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .020” X .020” DATE: 1/26/22**

**MFG: MOTOROLA THICKNESS .010” P/N: 2N4403**

**DG 10.1.2**

#### Rev B, 7/1